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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/669,159	09/25/00	CHEN H	TS2000-143

IM22/1228

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EXAMINER	
GOUDREAU, G	
ART UNIT	**PAPER NUMBER**
1763	3

DATE MAILED: 12/28/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09-669,159	Chen et. al
Examiner	**Group Art Unit**
George Goudreau	1763

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 (MONTH(S)) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on 9-00' (ie. - papers #1-2).

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-20 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☒ Claim(s) 17-20 is/are allowed.

☒ Claim(s) 1-6, 8-15 is/are rejected.

☒ Claim(s) 7, 16 is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received: _____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 2

☒ Notice of Reference(s) Cited, PTO-892

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other _____

Office Action Summary

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

17. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keller (5,346,586) further in view of Hills et. al. (5,382,316).

Keller discloses a process for patterning a W polycide gate using a process comprised of the following steps:

-A photo resist/ SiO2 hard mask/ W polycide/SiO2 laminate is formed on the surface of a Si wafer.;

-The photo resist is patterned, and used in the plasma etching of the SiO2 hard mask layer using a plasma comprised of (CF4-CHF3).;

-The WSi2 layer is plasma etched in a (SF6-He-O2) plasma using the patterned photo resist/ SiO2 hard mask as an etch mask.;

-The photo resist etch mask is removed from the wafer in-situ in the plasma etching chamber using O3 based plasma.; and

-The polysi layer is plasma etched using the SiO2 hard mask, and a plasma comprised of (HBr-Cl2).

This is discussed specifically in columns 3-8; and discussed in general in columns 1-8. This is shown in figures 1-2. Keller fails, however, to disclose the following aspects of applicant's claimed invention:

-the specific removal of the hard mask from the polysi layer after the polysi gate has been formed;

-the specific usage of a 2 step plasma etching process for patterning the polysi layer;

-the specific usage of an O2 based plasma to strip the photo resist etch mask after its usage;

-the specific usage of a plasma comprised of CF4 to remove etch polymers from the SiO2 hard mask after the hard mask has been etched but prior to the etching of the polysi layer; and

-the specific usage of a hard mask made out of SiON

Hills et. al. teach that it is desirable to simultaneously remove a photo resist etch mask, and etch polymers left on a polysi gate which was patterned in a previous plasma etching step by

employing a plasma comprised of (CF4-H2O-O2). This is discussed specifically in columns 2-3; and discussed in general in columns 1-6. This is shown in figures 1-2.

It would have been obvious to one skilled in the art to replace the O3 based plasma used to remove the photo resist etch mask in the etching process taught above with a plasma comprised of (CF4-H2O-O2) based upon the teachings of Hills et. al. that this is a desirable means for removing both a photo resist etch mask as well as polymeric etch residues left on a wafer from a previous plasma etching step. Further, this would simply involve the usage of an alternative, and at least equivalent means for removing the photo resist etch mask to those means specifically taught by Keller. (In this instance, the photo resist stripping step, and the SiO2 hard mask cleaning step would be comprised of the same process step since both processes occur at the same simultaneously.)

It would have been obvious to one skilled in the art to replace the SiO2 hard mask employed in the etching process taught above with a SiON hard mask based upon the following. The usage of SiON as a hard mask in the patterning of a polysi gate is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, this would simply represent the usage of an alternative, and at least equivalent means for providing a hard mask to be used in the patterning of a polysi layer to those means specifically taught.

It would have been obvious to one skilled in the art to remove the hard mask after the polysi gate has been patterned in the etching process taught above based upon the following. The

removal of a hard mask after it usage in the patterning of a gate electrode on a wafer is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, the hard mask would have had to been removed from the gate electrode after its formation in the process taught above in order to facilitate further processing of the wafer to form a device.

It would have been obvious to one skilled in the art to employ a two step plasma etching process to pattern the polysi layer in the etching process taught above based upon the following. The usage of a two step plasma etching process to pattern a polysi gate electrode layer on a wafer is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, this would have simply provided a means for reducing the amount of damage done to the SiO2 pad layer during the polysi etching step without significantly impairing the overall etching speed of the polysi layer by providing a low selectivity, high etching rate, first etch step followed by a high selectivity, low etching rate second, etch step for patterning the polysi layer on the SiO2 pad layer.

18. Claims 8-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the references as applied in paragraph 17 above further in view of Chapman (5,976,769).

The references as applied in paragraph 17 above fail to disclose the following aspects of applicant's claimed invention:

-the specific trimming of the width of the photo resist layer prior to using it to pattern the hard mask layer on polysi layer

Chapman teaches that it is desirable to employ a plasma comprised of (O2-He) to trim the width of patterned photo resist etch mask used to pattern a BARC layer in order to enhance the resolution of the etching process over that which is possible using prior art methods. The trimmed photo resist etch mask is then used in the anisotropic etching of a hard mask used to pattern a polysi layer on a wafer to form a polysi gate electrode. This is discussed specifically in columns 2-4; and discussed in general in columns 1-8. This is shown specifically in figures 2 a-2 h; and shown in general in figures 1-9.

It would have been obvious to one skilled in the art to trim the patterned photo resist etch mask after forming it but prior to using it to pattern the hard mask in the etching process taught above based upon the teachings of Chapman that it is desirable to do so in order to enhance the resolution of a dry etching process.

19. Claims 17-20 are allowed.

20. Claims 7, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner George A. Goudreau whose telephone number is (703) -308-1915. The examiner can normally be reached on Monday through Friday from 9:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Examiner Gregory Mills, can be reached on (703) -308-1633. The appropriate fax phone number for the organization where this application or proceeding is assigned is (703) -308-3599.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) -308-0661.

George A. Goudreau/gag

Examiner AU 1763